Refine Search

Search Results -

Terms	Documents
(semiconductor and memory and (charge adj trap$ adj layer) and diffus$ and bitline).clms.	0

Database:

> US Pre-Grant Publication Full-Text Database
> US Patents Full-Text Database
> US OCR Full-Text Database
> EPO Abstracts Database
> JPO Abstracts Database
> Derwent World Patents Index
> IBM Technical Disclosure Bulletins

Search: L10

[Refine Search]

[Recall Text] [Clear] [Interrupt]

Search History

DATE: Thursday, September 01, 2005   Printable Copy   Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=PGPB; PLUR=YES; OP=ADJ		
L10	(semiconductor and memory and (charge adj trap$ adj layer) and diffus$ and bitline).clms.	0	L10
	DB=JPAB; PLUR=YES; OP=ADJ		
L9	semiconductor and memory and (charge adj trap$ adj layer) and diffus$ and bitline	0	L9
	DB=EPAB; PLUR=YES; OP=ADJ		
L8	semiconductor and memory and (charge adj trap$ adj layer) and diffus$ and bitline	0	L8
	DB=USPT; PLUR=YES; OP=ADJ		
L7	semiconductor and memory and (charge adj trap$ adj layer) and diffus$ and bitline	32	L7
	DB=PGPB; PLUR=YES; OP=ADJ		
L6	semiconductor and memory and (charge adj trap$ adj layer) and diffus$ and bitline	23	L6
	DB=TDBD; PLUR=YES; OP=ADJ		

L5   semiconductor and memory and (charge adj trap$ adj layer) and diffus$ and bitline   0   L5

DB=DWPI; PLUR=YES; OP=ADJ

L4   semiconductor and memory and (charge adj trap$ adj layer) and diffus$ and bitline   0   L4

DB=PGPB; PLUR=YES; OP=ADJ

L3   semiconductor and memory and (charge adj trap$ adj layer) and diffus$ and bitlaine   0   L3

DB=TDBD; PLUR=YES; OP=ADJ

L2   semiconductor and memory and (charge adj trap$ adj layer) and diffus$ and bitlaine   0   L2

DB=DWPI; PLUR=YES; OP=ADJ

L1   semiconductor and memory and (charge adj trap$ adj layer) and diffus$ and bitlaine   0   L1

END OF SEARCH HISTORY